



## IN THE UNITED STATES PATENT & TRADEMARK OFFICE

SUBJECT:

Serial #:

10/614,928

File Date:

July 8, 2003

Inventor:

Jin-Yuan Lee

Examiner:

Menz, Douglas M.

Art Unit:

2891

Title: "A STRUCTURE OF HIGH PERFORMANCE COMBO

CHIP AND PROCESSING METHOD"

### **DECLARATION UNDER 37 CFR 1.131**

Honorable Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

## I, Jin-Yuan Lee, hereby state:

- 1. I am the inventor of Claims 25-45 of the above-identified patent application.
- 2. Prior to Dec. 4, 2000, I conceived of the idea for the electronic package as described and claimed in my application, and a copy of the invention disclosure describing my invention entered the United States of America before Dec. 4, 2000. The invention disclosure including drawings shows my invention as claimed in Claims 25-29, 31-35, and 45 and is attached as Exhibit A. Each of the dates blanked out from Exhibit A is prior to Dec. 4, 2000.

MEG00-009B Serial no. 10/614,928

3. A first draft of the patent application was sent to me by George O. Saile & Associates on September 18, 2000. A copy of the letter accompanying the draft is attached as Exhibit B.

- A second draft of the patent application was sent to me by George O. Saile &
  Associates on Dec. 8, 2000. A copy of the mail log of George O. Saile & Associates
  for Dec. 8, 2000 is attached as Exhibit C.
- 5. I returned the second draft of the patent application to George O. Saile & Associates. A copy of their mail log shows the draft was received by them on June 25, 2001. The mail log is attached as Exhibit D.
- 6. A final draft of the patent application was sent to me by email on July 27, 2001. A copy of the email letter accompanying the copy is attached as Exhibit E.
- 7. The patent application serial number 09/953,544, to which the instant patent application claims priority, was constructively reduced to practice by on September 17, 2001.
- 8. These exhibits show conception prior to the effective date of the reference plus diligence from prior to the reference date of Dec. 4, 2000 to constructive reduction to practice on September 17, 2001.

MEG00-009B Serial no. 10/614,928

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Jin-Yuan Lee Jun-13, 2006 Jin-yuan Lee Date

Confidential (When Completed)

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Full Name(s	) of Inventor(s)	Employee	Department	Dept.	Tel No.	For Use by IP Law
English	Chinese	No.		Code		Disclosure No.
Jin-yuan Lee	李進源					2000-009
<u> </u>	林茂雄					Received Date:
	1,110					(Time Stamp)
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Title of Invention -

- · English: A structure of high performance combo chip and processing method
- Chinese:

Background Information - Current Practice and Disadvantages

Currently, high performance combo chip is in MCM (multiple chip module) or MCP (multiple chip package) format. The disadvantages of MCM and MCP are higher cost and bigger package size.

Main Points of Claim (Please List Item by Item)

- 1. Combining multiple chips face to face
- 2. I/Os of combo chip are ball grid array on the bottom of top chips.
- 3. Wafer level processing

Problem Solved or Improvements Obtained by this Invention (Please List Item by Item)

- 1. High performance system on chip can be achieved by combining multiple chips face to face.
- 2. Smaller package size
- 3. It can be Lower manufacturing cost because of wafer level processing

Keyword Search for Patent/Literatures

Patent/Literatures Search Result (Please Specify Similar Patent No. and Literature Con-16 200

Detailed Description of Invention - (Continued Next Page)

Disclosure Submitted by Witnesses: The Two Witnesses whose Signatures appear below Inventor's Signature Date Inventor's Signature Date have Read and Understand this Entire Invention Disclosure. Jin Tuan Lel Signature of Witness Date Inventor's Signature Date Inventor's Signature Date Signature of Witness Date

invention Disclosure of Megic		Confidential (When Completed)
Detailed Description of Inventi-	on – Continued	For Use by IP Lav
	·	Disclosure No.
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	Inventor's Signature Date	Inventor's Signature Date
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Invention Disclosure of Megic C		fidential (When Completed)
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whose Signatures appear below have Read and Understand this Entire Invention Disclosure.  Signature of Witness Date  J Chan		Inventor's Signature Date  Inventor's Signature Date
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Invention Disclosure of Megic (	Corp. Page 6 of 7 Confi	dential (When Completed)
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Signature of Witness Date	Inventor's Signature Date	Inventor's Signature Date
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Detailed Description of Invention – Continued  For Use by IP Law Disclosure No.  2000 – 009  11. Flip-chip BGA package formation  * Combo chip BGA package performed by conventional flip-chip assembly  Underfill of flip-chip BGA  PCB substrate  PCB substrate  PCB substrate  Disclosure Submitted by  whose Signatures appear below have Read and Understand this  Inventor's Signature Date  Inventor's Signature Date	Invention Disclosure of Megic	Corp. Page 7 of 7 Confi	dential (When Completed)
Witnesses: The Two Witnesses whose Signatures appear below have Read and Understand this Entire Invention Disclosure.  Signature of Witness Date  T. J. Cham.  11. Flip-chip BGA package formation  * Combo chip BGA  PCB substrate  PCB substrate  PCB substrate  Inventor's Signature Date	Detailed Description of Invention	n – Continued	
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Witnesses: The Two Witnesses whose Signatures appear below have Read and Understand this Entire Invention Disclosure.  Signature of Witness Date  T. J. Chan Inventor's Signature Date	11. Flip-chip BGA package *. Combo chip BGA	formation package performed by conventional flip-c	hip assembly
Witnesses: The Two Witnesses whose Signatures appear below have Read and Understand this Entire Invention Disclosure.  Signature of Witness Date  T. J. Chan  Disclosure Submitted by  Inventor's Signature Date	Underfill of flip-chip		PCB substrate
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# GEORGE O. SAILE & ASSOCIATES 20 MCINTOSH DRIVE POUGHKEEPSIE, NY 12603

September 18, 2000

TO:

M.S. Lin

MEGIC Corp.

FROM:

Stephen B. Ackerman

Fax: 914 4712064

Subject:

Patent Application Reference MEG 2000-009

Inventor:

J.Y. Lee

Please have the Inventor review the enclosed Draft Patent Application. He should make any changes he sees fit, answer all of our questions, and fill in the blanks. The Declaration and Assignment are enclosed for his completion. Please complete the attached Small Entity Form. Review the Drawings carefully for any errors AND ADDITIONS. This is the time when we have the best opportunity to make the description of the invention complete and correct.

Please return the corrected description and Drawing as soon as you can.

With Best Regards,

Stephen B. Ackerman



## ExhibitC

## Dockets Sent

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To: Chris Wang, Megic, INTERNET:chrishwang@megic.com.tw

From: Stephen Ackerman, 102706,1346

Date: 7/27/2001, 11:51 AM Re: MEG00-009 and -010

Hi Chris,

Here are the final versions of the text of MEG00-009 and MEG00-010. Drawings and papers for signing are being sent separately by fax.

With best regards, Steve